Amendments to the Claims

This listing of claims will replace all prior versions and listings of claim in the application.

1) (currently amended) A phase locked loop circuit, comprising:

a phase-frequency detector ~~capable of providing~~ to provide a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, ~~capable of providing~~ to provide a first voltage ~~responsive~~ in response to the phase difference signal;

a filter, coupled to the charge-pump, ~~capable of providing~~ to provide a second voltage ~~responsive~~ in response to the first voltage;

a first voltage-controlled oscillator, coupled to the filter, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the second voltage; and,

a second voltage-controlled oscillator, coupled to the filter, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the second voltage,

wherein the charge-pump includes a gain that is adjustable in response to a control signal.

2) (currently amended) The phase locked loop circuit of claim 1, further comprising:

a multiplexer, coupled to the first and second voltage-controlled oscillators, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to ~~a~~ the control signal.

3) (cancelled)

4) (currently amended) The phase locked loop circuit of claim 1~~3~~, wherein the ~~adjustable~~ gain corresponds to a current that is adjustable.

5) (currently amended) The phase locked loop circuit of claim 1, wherein the filter includes ~~an adjustable~~ a resistor having a resistance that is adjustable ~~responsive~~ in response to ~~a~~ the control signal.

6) (currently amended) The phase locked loop circuit of claim 1, further comprising:

a multiplexer, coupled to the first and second voltage-controlled oscillators, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to ~~a~~ the control signal,

~~wherein the charge pump includes an adjustable gain responsive to the control signal,~~

wherein the filter includes ~~an adjustable~~ a resistor having a resistance that is adjustable ~~resistor responsive~~ in response to the control signal.

7) (currently amended) The phase locked loop circuit of claim 1, further comprising:

a voltage regulator, coupled to the filter and the first and second voltage-controlled oscillators, ~~capable of providing~~ to provide the second voltage.

8) (previously presented) The phase locked loop circuit of claim 7, wherein the voltage regulator includes an operational amplifier.

9) (previously presented) The phase locked loop circuit of claim 1, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

10) (previously presented) The phase locked loop circuit of claim 1, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

11) (previously presented) The phase locked loop circuit of claim 1, wherein the filter includes a low-pass filter.

12) (previously presented) The phase locked loop circuit of claim 1, wherein the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit.

13) (previously presented) The phase locked loop circuit of claim 12, wherein the phase locked loop circuit, the serializer circuit and deserializer circuit are included in a memory device.

14) (currently amended) A phase locked loop circuit, comprising:

a phase-frequency detector ~~capable of providing~~ to provide a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, ~~capable of providing~~ to provide a first voltage ~~responsive~~ in response to the phase difference signal;

a filter, coupled to the charge-pump, ~~capable of providing~~ to provide a second voltage ~~responsive~~ in response to the first voltage;

an amplifier, coupled to the filter, ~~capable of providing~~ to provide a buffered voltage ~~responsive~~ in response to the second voltage;

a multiplexer, coupled to the amplifier, ~~capable of providing~~ to provide the buffered voltage ~~responsive~~ in response to a control signal;

a first voltage-controlled oscillator, coupled to the multiplexer, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the buffered voltage; and,

a second voltage-controlled oscillator, coupled to the multiplexer, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the buffered voltage.

15) (currently amended) The phase locked loop circuit of claim 14, wherein the charge-pump includes ~~an adjustable~~ a gain that is adjustable in response ~~responsive~~ to the control signal.

16) (currently amended) The phase locked loop circuit of claim 15, wherein the ~~adjustable~~ gain corresponds to a current that is adjustable.

17) (currently amended) The phase locked loop circuit of claim 14, wherein the filter includes ~~an adjustable~~ a resistor having a resistance that is adjustable in response ~~responsive~~ to the control signal.

18) (previously presented) The phase locked loop circuit of claim 14, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

19) (previously presented) The phase locked loop circuit of claim 14, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

20) (previously presented) The phase locked loop circuit of claim 14, wherein the filter includes a low-pass filter.

21) (previously presented) The phase locked loop circuit of claim 14, wherein the phase locked loop circuit is coupled to a serializer circuit and a deserializer circuit.

22) (previously presented) The phase locked loop circuit of claim 21, wherein the phase locked loop circuit, the serializer circuit and deserializer circuit are included in a memory device.

23) (currently amended) A phase locked loop circuit, comprising:

a phase-frequency detector ~~capable of providing~~ to provide a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal;

a charge-pump, coupled to the phase-frequency detector, ~~capable of providing~~ to provide a first voltage ~~responsive~~ in response to the phase difference signal;

a filter, coupled to the charge-pump, ~~capable of providing~~ to provide a second voltage ~~responsive~~ in response to the first voltage;

a first amplifier, coupled to the filter, ~~capable of providing~~ to provide a first buffered voltage ~~responsive~~ in response to the second voltage;

a second amplifier, coupled to the filter, ~~capable of providing~~ to provide a second buffered voltage ~~responsive~~ in response to the second voltage;

a first voltage-controlled oscillator, coupled to the first amplifier, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the first buffered voltage; and,

a second voltage-controlled oscillator, coupled to the second amplifier, ~~capable of providing~~ to provide the feedback signal ~~responsive~~ in response to the second buffered voltage.

24) (currently amended) The phase locked loop circuit of claim 23, wherein the charge-pump includes ~~an adjustable~~ a gain that is adjustable in response ~~responsive~~ to a control signal.

25) (currently amended) The phase locked loop circuit of claim 24, wherein the ~~adjustable~~ gain corresponds to a current that is adjustable.

26) (previously presented) The phase locked loop circuit of claim 23, wherein the filter includes ~~an adjustable~~ a resistor having a resistance that is adjustable in response ~~responsive~~ to a control signal.

27) (currently amended) The phase locked loop circuit of claim 23,

wherein the first amplifier is operational ~~responsive~~ in response to a control signal,

wherein the second amplifier is operational ~~responsive~~ in response to the control signal,

wherein the charge-pump includes ~~an adjustable~~ a gain that is adjustable in response ~~responsive~~ to the control signal,

wherein the filter includes ~~an adjustable~~ a resistor having a resistance that is adjustable in response ~~responsive~~ to the control signal.

28) (previously presented) The phase locked loop circuit of claim 23, further comprising:

a phase mixer coupled to the first and second voltage-controlled oscillators.

29) (previously presented) The phase locked loop circuit of claim 23, further comprising:

a clock buffer coupled to the first and second voltage-controlled oscillators.

30) (previously presented) The phase locked loop circuit of claim 23, wherein the filter includes a low-pass filter.

31) (currently amended) A method, comprising:

obtaining a phase difference signal ~~responsive~~ in response to an input signal and a feedback signal; and,

providing an adjustable frequency range for the feedback signal ~~responsive~~ in response to a first control signal,

wherein the providing includes adjusting a current in a charge-pump.

32) (previously presented) The method of claim 31, wherein a phase locked loop circuit performs the method.

33) (cancelled)

34) (previously presented) The method of claim 31, wherein the providing includes adjusting a resistance in a filter.

35) (previously presented) The method of claim 31, wherein the providing includes selecting an output of a multiplexer.

36) (previously presented) The method of claim 31, wherein the providing includes selecting an operation of an amplifier.

37) (currently amended) The method of claim 31, wherein the providing comprises:
providing ~~a~~ the first control signal to ~~a~~ the charge-pump;
providing a second control signal to a filter; and,
providing a third control signal to a multiplexer.

38) (currently amended) A circuit, comprising:

a phase locked loop circuit ~~capable of providing~~ to provide an output signal

~~responsive~~ in response to a comparison of an input signal and the output signal; and,

means, coupled to the phase locked loop circuit, for adjusting a frequency range of the output signal ~~responsive~~ in response to a control signal,

wherein the means includes adjusting a current in a charge-pump in response to the control signal.